LogicGates, Transistors & its Applications

1 Mark Questions

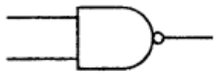
1.In a transistor, doping level in base is increased slightly. How will it affect
(i)collector current and
(ii)base current? [Delhi 2011]

Ans.(i) Collector current decreases.
(ii) Base current increases

2.Draw the logic circuit of a NAND gate and write its truth table.[Foreign 20113]

Ans.

Logic circuit of a NAND gate



Truth table

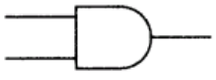
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

3.Draw the logic circuit of AND gate and write its truth table.[Foreign 2011]

Ans.

Logic circuit of a AND gate



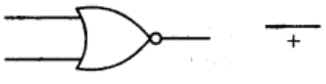
Truth table

A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

4.Draw the logic circuit of NOT gate and write its truth table.[Foreign 2011]

Ans.

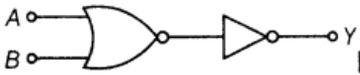
Logic circuit of a NOT gate



Truth table

A	$Y = \overline{A}$
0	1
1	0

5. Write the truth table for the following circuit. Name the equivalent gate that this circuit represents.



[Foreign 2010]

Ans.

The given combination consists of NOR gate and NOT gate, so equivalent gate is OR gate.

Truth table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

(1/2 × 2 = 1)

From the truth table, it is clear that the output is 1 only when at least one of the inputs is at the high state i.e. 1

6. The truth table of a logic gate has the form given here. Name this gate and draw its symbol.

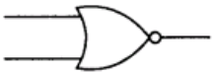
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

[All India 2010C]

Ans.

Logic gate is NOR gate.

Symbol



7. The truth table of a logic gate has the form given here. Name this gate and draw its symbol.

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

[All India 2010C]

Ans.

Logic circuit of a NAND gate

Truth table

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

8.Give the logic symbol of NOR gate.[All India 2009]

Ans.

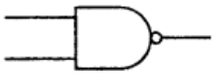
Logic gate is NOR gate.

Symbol

9.Give the logic symbol of NAND gate. [All India 2009]

Ans.

Logic circuit of a NAND gate



Truth table

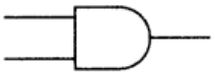
A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

10.Give the logic symbol of AND gate.[All India 2009]

Ans.

Logic circuit of a AND gate



Truth table

A	B	$Y = AB$
0	0	0
0	1	0
1	0	0
1	1	1

11.Define current amplification factor in common-emitter mode of transistor. [Delhi 2009 C, All India 2010 C]

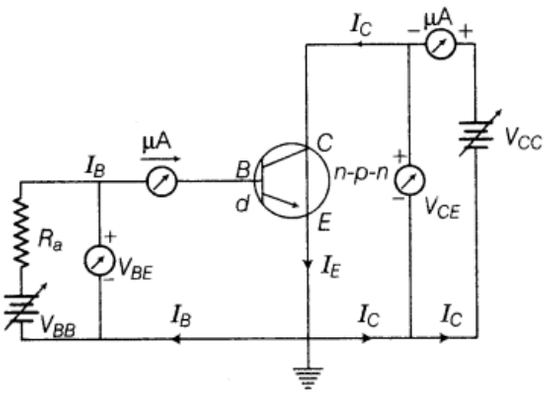
Ans.

Current amplification factor in common emitter mode, $\beta_{AC} = \left|\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}}$ **(1)**

2 Marks Questions

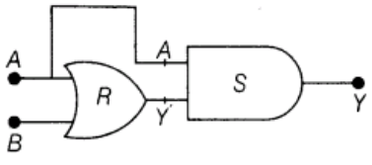
12.Draw a circuit diagram of n-p-n transistor amplifier in CE configuration. Under what condition does the transistor act as an amplifier? [All India 2014]

Ans. Circuit diagram of n-p-n transistor amplifier in CE configuration is given below



The condition for the amplifier to work is that the base-emitter junction should be forward biased and collector-base junction should be reversed biased

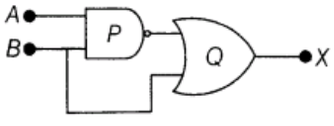
13. Write the truth table for the combination of the gates shown. Name the gates used. **[All India 2014]**



Ans.

A	B	$Y' = A + B$	$Y = A \cdot (A + B)$
0	0	0	0
0	1	1	0
1	0	1	1
1	1	1	1

14. Identify the logic gates marked P and Q in the given circuit. Write the truth table for the combination.



[Delhi 2014]

Ans.

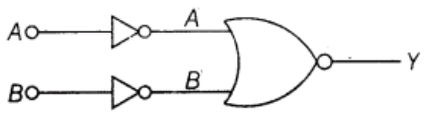
The logic gates are Pis NAND gate and Q is OR gate.

The truth table is given as shown in below:

A	B	$A \cdot B$	$\overline{A \cdot B}$	$X = B + \overline{A \cdot B}$
0	0	0	1	1
0	1	0	1	1
1	0	0	1	1
1	1	1	0	1

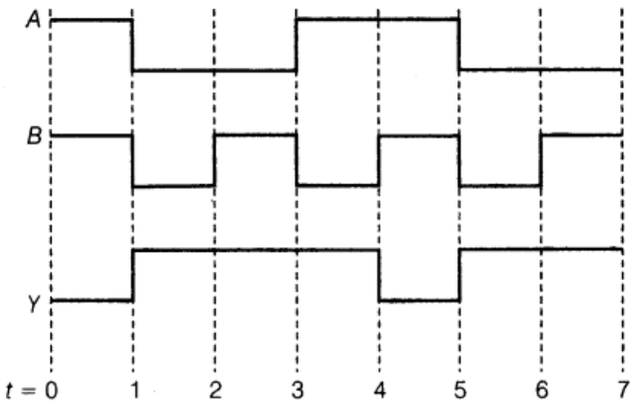
15.The outputs of two NOT gates are fed to a NOR gate. Draw the logic circuit of the combination of gates. Give its truth table. Identify the gate represented by this combination. [Delhi 2014 C]

Ans.



16.The input wave forms A and B and the output waveform Y of a gate are shown below. Name the gate it represents, write its truth table and draw the logic symbol of this gate.

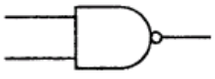
represents, write its truth table and draw the logic symbol of this gate.



[All India 2014C]

Ans.

Logic circuit of a NAND gate

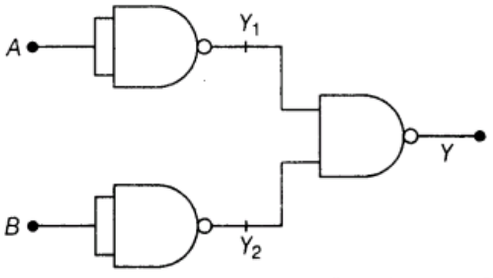


Truth table

A	B	$Y = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

(1/2 × 2 = 1)

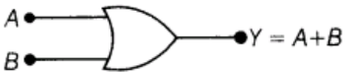
17. Identify the equivalent gate represented by the circuit shown in the figure. Draw its logic symbol and write the truth table.



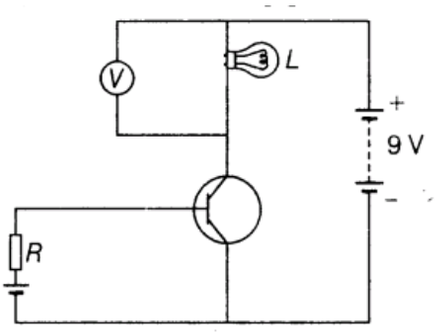
[Foreign 2014]

Ans.

and logic symbol is



18.In the given circuit diagram, a voltmeter V is connected across a lamp L. How would
(i)the brightness of the lamp and
(ii)voltmeter reading V be affected if the value of resistance R is decreased? Justify your answer.



Ans.

The given figure in question is common-emitter (*CE*) configuration of an *n-p-n* transistor. The input circuit is forward biased and collector circuit is reverse biased. **(1)**

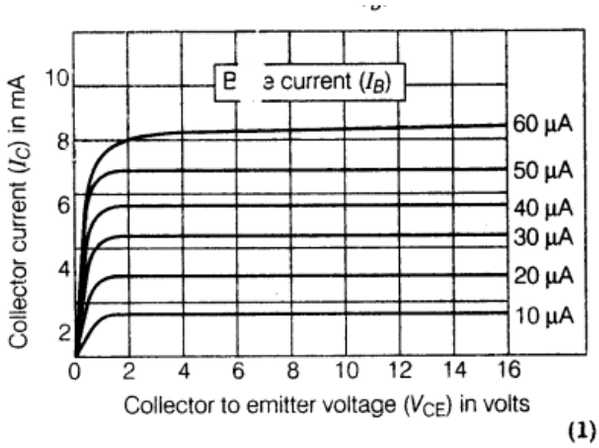
As, the base resistance *R* decreases, the input circuit will become more forward biased thus, decreasing the base current (I_B) and increasing the emitter current (I_E). This will increase the collector current (I_C) as $I_E = I_B + I_C$.

When I_C increases which flows through the lamp, the voltage across the bulb will also increase thus making the lamp brighter and as the voltmeter is connected in parallel with the lamp, the reading in the voltmeter will also increases. **(1)**

19.Draw a typical output characteristics of an n-p-n transistor in CE Show how these characteristics can be used to determine output resistance?[All India 2013]

Ans.

Output characteristics is the plot between collector-emitter voltage (V_{CE}) and the collector current (I_C) at different constant values of base current (I_B).

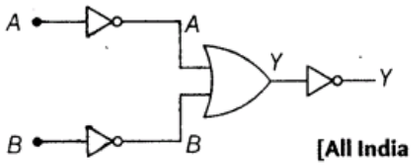


(1)

Output resistance is defined as the ratio of variation of collector-emitter voltage (ΔI_C) and corresponding change in collector current (ΔI_C) when base current remains constant. Initially with the increase in V_{CE} the collector current increases almost linearly, this is because the junction is not reverse biased. When the supply is more than required to reverse bias, the base-collector junction, i_C increases very little with V_{CE}.

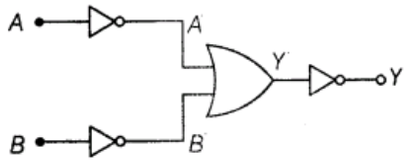
The reciprocal of slope of the linear part of the curve gives the value of output resistance, i.e. $r_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$ **(1)**

20. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.



$A' = \overline{A}, B' = \overline{B}$

$Y' = A'B'$

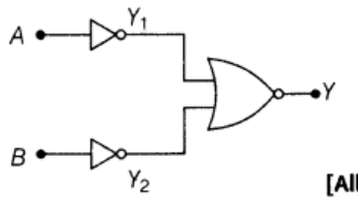
$Y = \overline{Y'} = \overline{A' + B'} \Rightarrow = \overline{\overline{A}.\overline{B}} = A.B$ **(1)**

The equivalent gate of the given circuit is AND gate.

Truth table

A	B	A′	B′	Y′	Y
1	1	0	0	0	1
1	0	0	1	1	0
0	1	1	0	1	0
0	0	1	1	1	0

21. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.

$Y_1 = \bar{A}$ and $Y_2 = \bar{B}$

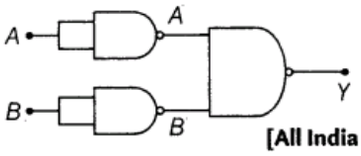
$\therefore \quad Y = \overline{Y_1 + Y_2} = \bar{Y}_1 . \bar{Y}_2 = \bar{\bar{A}} . \bar{\bar{B}} = A.B$

The equivalent gate of the given circuit is AND gate. **(1)**

Truth table

A	B	Y_1	Y_2	Y
1	1	0	0	1
1	0	0	1	0
0	1	1	0	0
0	0	1	1	0

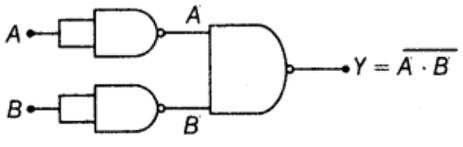
22. In the circuit shown in the figure, identify the equivalent gate of the circuit and make its truth table.



[All India 2013]

Ans.

$Y = \overline{A' \cdot B'} = \bar{\bar{A}} + \bar{\bar{B}} = A + B$



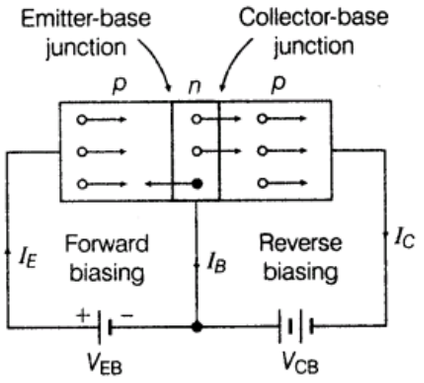
Truth table

A	B	$A' = \overline{A \cdot A}$	$B' = \overline{B \cdot B}$	$Y = \overline{A \cdot B}$ $= A + B$
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Thus, the equivalent gate is OR gate. **(1)**

23.Describe briefly with the help of a circuit diagram, how the flow of current carriers in a p-n-p transistor is regulated with emitter-base junction in forward biased and base-collector junction in reverse biased. [All India 2012]

Ans.

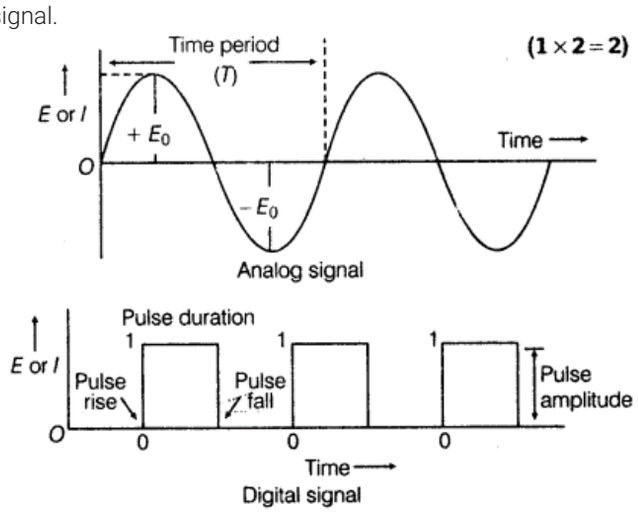


Heavily doped emitter is subjected to electric field by emitter-base battery and consequently, holes gets drifted towards collector through thin and lightly doped base region. Nearly 5% hole, which drifted from emitter combined with electron in base region and remaining nearly 95% hole reaches to collector under the influence V_{CE}.

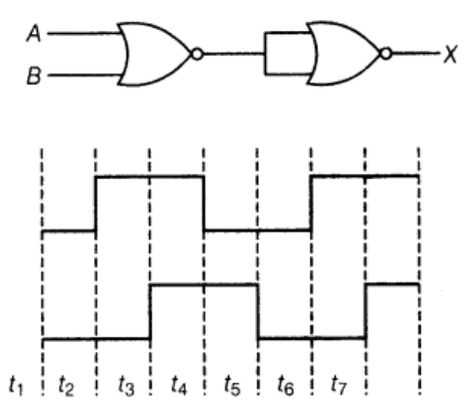
24.Distinguish between analog signal and digital signal. [All India 2012]

Ans.A signal in which current or voltage changes continuously with the time is called analog signals. A signal in which current or voltage can take only two discrete values is called a digital signal.

(1 × 2 = 2)



25.Draw the output waveform at X using the given inputs, A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit

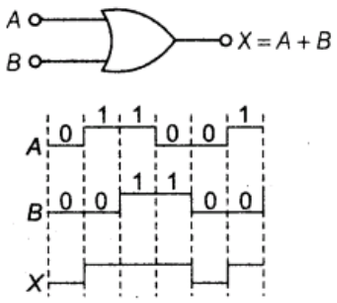


[Delhi 2012; 2011]

Ans. Equivalent gate is OR gate. If input A or B or both are 1, then the output of OR gate is 1.

Boolean expression of OR gate is given as A + B = X

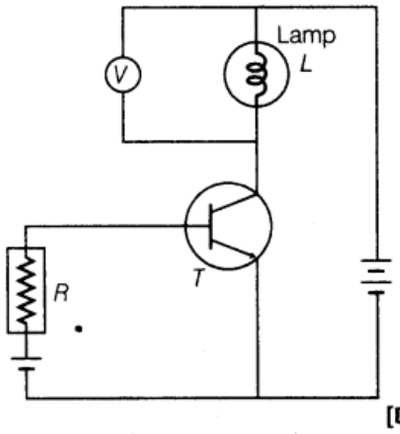
Logic symbol of OR gate and the output waveform as shown below



Truth table

Inputs		Output
A	B	$X = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

26.In the given circuit, a voltmeter V is connected across lamp L What changes would you observe in the lamp L and the voltmeter V if the value of resistor R is reduced?

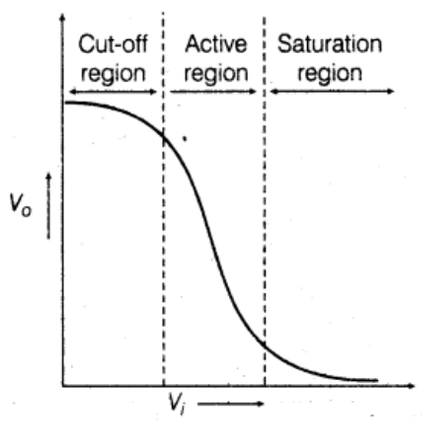


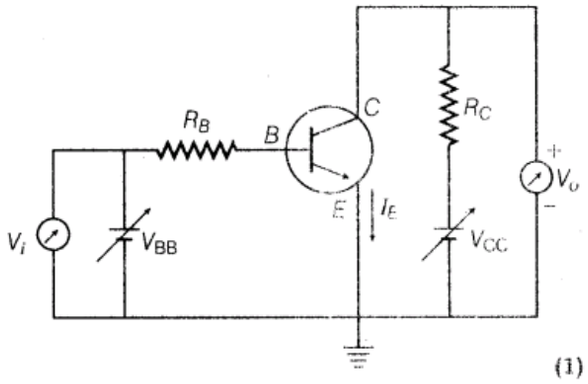
[Delhi 2011C]

Ans. Lamp glows brighter and voltmeter reading increases with the decrease of R. Input current increase which in turn by transistor action lead to increase collector current. This makes lamp brighter and hence, voltmeter reading goes up.

27.Draw the transfer characteristic curve of a base-biased transistor in CE Explain clearly how the active region of the V_0 versus Vi. curve, in a transistor is used as an amplifier? [Delhi 2011]

Ans.The transfer characteristic curve of base biased transistor in CE configuration as shown below:





(1)

As, V_i increases slightly above 0.6 V, a current I_C flows in the output circuit and the transistor arrives in active state.

$$\therefore \qquad V_o = V_{CC} - I_C R_C$$

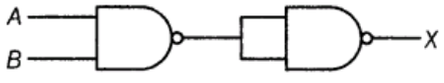
with the growth of I_C, V_C decrease linearly.

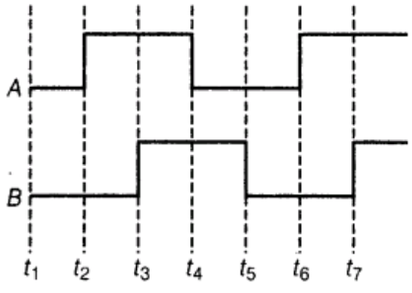
Also, voltage gain in active state is given by

$$A_V = -\frac{\Delta V_o}{\Delta V_i} \qquad (\because \Delta V_o > \Delta V_i)$$

There is voltage gain and hence amplification of voltage takes place. Thus, transistor used as an amplifier. (2)

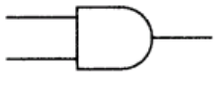
28.Draw the output waveform at X using the given inputs, A and B for the logic circuit shown below. Also, identify the logic operation performed by this circuit.[Delhi 2011; 2008]





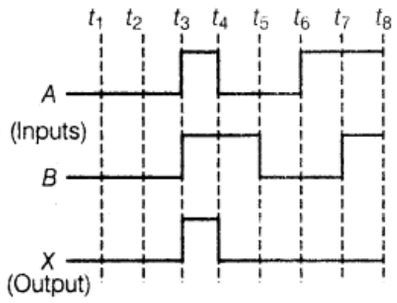
Ans.

Logic circuit of a AND gate



Truth table

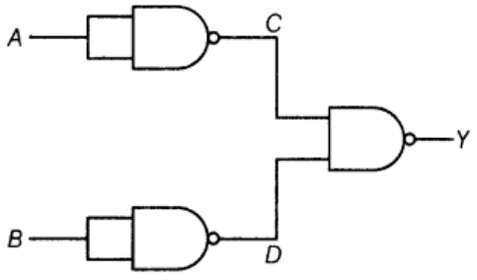
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1



Logic operation of the graphic circuit

$$X = \overline{\overline{A \cdot B}} = AB$$

29.Write the truth table for the logic circuit shown below and identify the logic operation performed by this Circuit. [Delhi 2011]



Ans.

The truth table of given system is as follows:

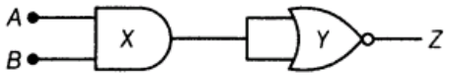
(1/2)

A	B	$C = A \cdot \bar{A}$	$D = \bar{A} \cdot B$	$Y = \bar{C} \cdot D$
0	0	1	1	0
1	1	0	0	1
1	0	0	1	1
0	1	1	0	1

(1½)

The correct performs the logic operation of OR gate.

30.Identify the logic gates X and Y in the figure. Write down the truth table of output Z for all possible inputs A and [All India 2011 c]



Ans.

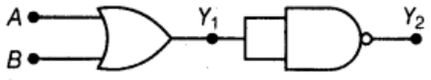
X : AND gate

Y : NOT gate

Z : $Y = \overline{A \cdot B}$

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

31. (*i*) For the digital circuit given below, write the truth table showing outputs Y_1 and Y_2 for all possible inputs of A and B.



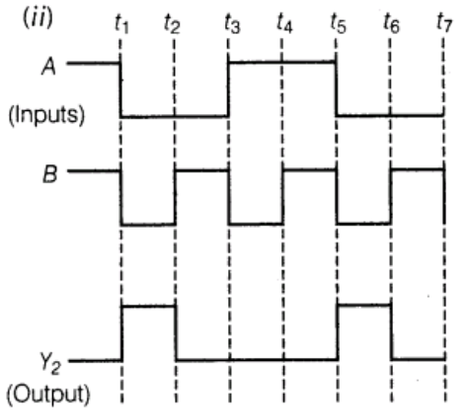
(ii) Show output waveform for all possible inputs of A and B.[All India 2011 C]

Ans.

(*i*) As, $Y_1 = A + B$, $Y_2 = \overline{A + B}$

A	B	Y_1	Y_2
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(*ii*)

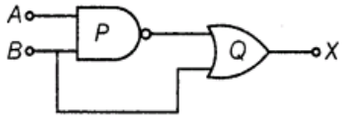


32. (*i*) Identify the logic gates marked P and Q in the given logic circuit.

(*ii*) Write down the output at X for the inputs,

$A = 0, B = 0$ and $A = 1, B = 1$.

[All India 2010]



Ans.

(*i*) P : NAND gate

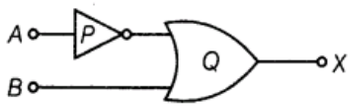
Q : OR gate

(*ii*) $X = \overline{A \cdot B} + B$ **(1/2 × 2 = 1)**

For $A = 0, B = 0, X = \overline{0.0} + 0 = 1 + 0 = 1$

For $A = 1, B = 1, X = \overline{1.1} + 1 = 0 + 1 = 1$h. **(1)**

33. (*i*) Identify the logic gates marked *P* and *Q* in the given logic circuit.



(*ii*) Write down the output at *X* for the inputs $A = 0, B = 0$ and $A = 1, B = 1$, **[All India 2010]**

Ans.

(*i*) *P* : NOT gate and *Q* : OR gate

(*ii*) $X = (\overline{A} + B)$ **(1/2 × 2 = 1)**

For $A = B = 0$, $X = \overline{0} + 0 = 1 + 0 = 1$

For $A = 1, B = 1$, $X = \overline{1} + 1 = 0 + 1 = 1$ **(1)**

34. Define the following terms.

(*i*) Input resistance r_i.

(*ii*) Current amplification factor β of a transistor used in its *CE* configuration. **[All India 2010C]**

Ans.

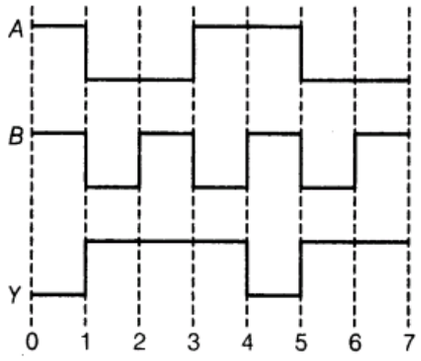
(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$ **(1)**

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$ **(1)**

35. The following figure shows the input waveforms A, B and the output waveform Y of a gate. Identify the gate, write its truth table and draw its logic symbol. **[Delhi 2009]**



Ans.

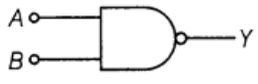
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

(1)

Logic symbol



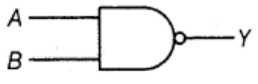
$Y = \overline{A \cdot B}$ **(1/2)**

36.The output of a 2-input AND gate is fed to a NOT gate. Give the name of the combination and its logic symbol. Write down its truth table.[Foreign 2008, Delhi 2009]

Ans.

When output of a two inputs AND gate is fed to a NOT gate, then the combination is called NAND gate

Logic symbol



(1)

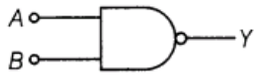
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

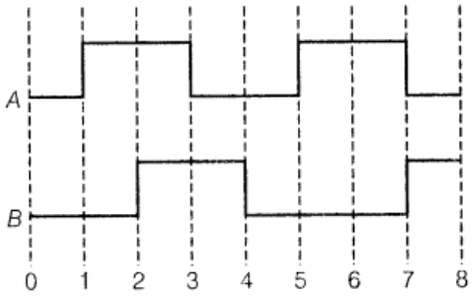
(1)

Logic symbol



$Y = \overline{A \cdot B}$ **(1/2)**

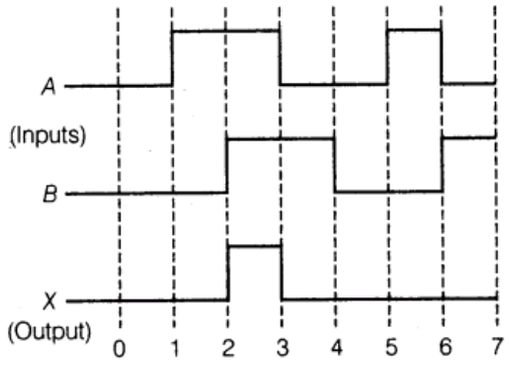
37. (*i*) Sketch the output waveform from an AND gate for the inputs, *A* and *B* shown in the figure.



(*ii*) If the output of the above AND gate is fed to a NOT gate, name the gate of the combination, so formed. **[Delhi 2009]**

Ans.

(*i*) Output of AND gate is $Y = A \cdot B$. In this case, output will be 1 only when both inputs are 1.



38. Draw the logic symbol of the gate whose truth table is given as below:

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If this, logic gate is connected to NOT gate, what will be the output when

(i)A = 0, B = 0 and

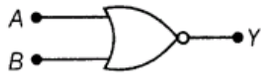
(ii)A = 1 B = 1?

Draw the logic symbol of the Combination.[Foreign 2009]

Ans.

NOR gate

Symbol



(1)

On connecting the given gate with NOT gate, the output

$$Y = \overline{\overline{A + B}} = A + B$$

(*i*) If $A = 0, B = 0 \Rightarrow Y = A + B = 0 + 0 = 0$

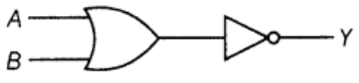
(*ii*) If $A = 1, B = 1$

$Y = 1 + 1 = 1.$ **(1)**

39.A logic gate is obtained by applying output of OR gate to a NOT gate.Name the gate so formed. Write the symbol and truth table of this gate.[Foreign 2009]

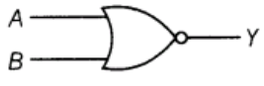
Ans.

Logic gate



Equivalent so formed gate is NOR gate.

Symbol



(1)

Truth table $Y = \overline{A + B}$

A	$\bar{A}$	B	$\bar{B}$	$Y = \bar{A} \cdot \bar{B}$
0	1	0	1	1
0	1	1	0	0
1	0	0	1	0
1	0	1	0	0

40.A logic gate is obtained by applying output of AND gate to a NOT gate. Name the gate so formed. Write the symbol and truth table of this gate.[Foreign 2009]

Ans.

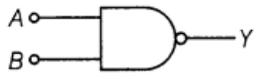
Gate From the given output waveform, it is clear that output is zero only when both inputs are 1, so the gate is NAND gate. **(1/2)**

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

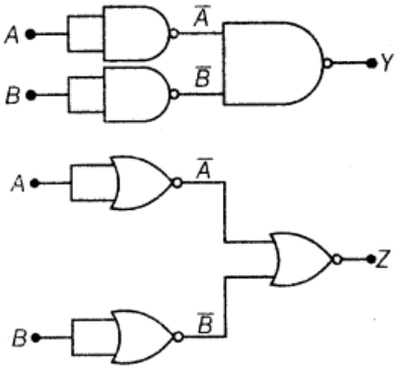
(1)

Logic symbol



$Y = \overline{A \cdot B}$ **(1/2)**

41.The two circuits shown here are a combination



(i)Three NAND gates.

(ii)Three NOR gates.

Write truth tables for each of these combinations. [Delhi 2009 c]

Ans.

(*i*)

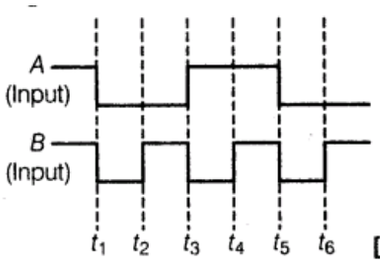
A	$\overline{A}$	B	$\overline{B}$	$Y = \overline{\overline{A} + \overline{B}} = A + B$
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1

(1)

(*ii*)

A	$\overline{A}$	B	$\overline{B}$	$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$
0	1	0	1	0
0	1	1	0	0
1	0	0	1	0
1	0	1	0	1

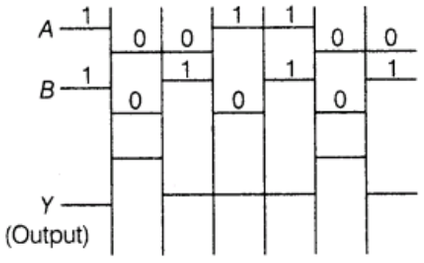
42.The given inputs A, B are fed to a 2-input NAND gate. Draw the output waveform of the gate.



[Delhi 2008]

Ans.

Output of NAND gate is $Y = \overline{A \cdot B}$, the output will be 1 only when both inputs are zero.



(2)

43.In the output of a 2-input NOR gate is fed as both inputs, A and B to another NOR gate, write down a truth table to find the final output, for all combinations of A, B.[Delhi 2008]

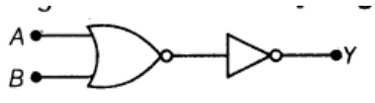
Ans.

Equivalent gate is OR gate.

Truth table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

44.Write the truth table and draw the logic symbol of the gate for the circuit given as below: [Foreign 2008]



Ans.

Equivalent gate is OR gate.

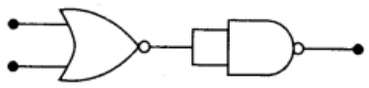
Symbol

Truth table

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

45. Write the truth table and draw the logic symbol of the gate for the circuit given as below:

[Foreign 2008]



Ans.

Equivalent gate is AND gate

Symbol

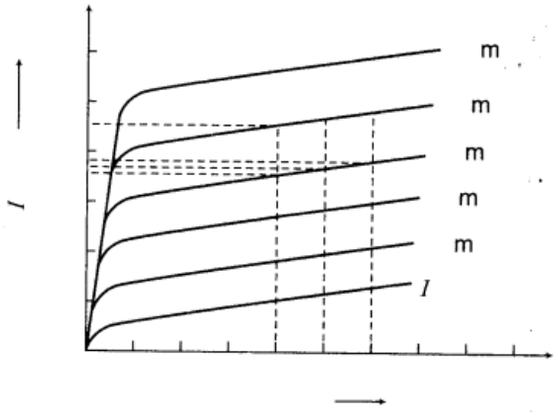
AND gate

Truth table

A	B	Y = A
0	0	0
0	1	0
1	0	0
1	1	1

3 Marks Questions

46.Output characteristics of an n-p-n transistor in CE configuration is -shown in the figure. Determine



(*i*) dynamic output resistance
(*ii*) DC current gain and
(*iii*) AC current gain at an operating point $V_{CE} = 10$ V, when $I_B = 30$ μA. **[Delhi 2013]**

Ans.

(*i*) Dynamic output resistance is given as

$$R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}} = \frac{12 - 8}{(3.6 - 3.4) \times 10^{-3}}$$

$$= \frac{4}{0.2 \times 10^{-3}} = 20\ \text{k}\Omega \quad \textbf{(1)}$$

(*ii*) DC current gain,

$$\beta_{DC} = \frac{I_C}{I_B} = \frac{3.5\ \text{mA}}{30\ \mu\text{A}} = \frac{3.5 \times 10^{-3}}{30 \times 10^{-6}}$$

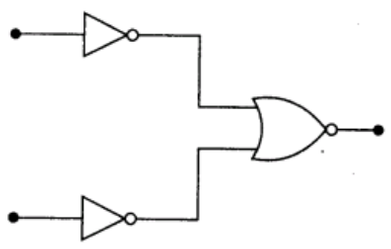
$$= \frac{350}{3} = 116.67 \quad \textbf{(1)}$$

(*iii*) AC current gain,

$$\beta_{DC} = \frac{\Delta I_C}{\Delta I_B} = \frac{(4.7 - 3.5)\,mA}{(40 - 30)\,\mu A}$$

$$= \frac{1.2 \times 10^{-3}}{10 \times 10^{-6}} = 120$$

47.You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate which Corresponds to [All India 2011]



Ans.

Truth table of given circuit is as shown below:

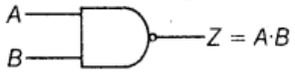
A	B	$X = \bar{A}$	$Y = \bar{B}$	$Z = \overline{X + Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem

$$Z = \overline{X + Y} = \overline{\bar{A} + \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B = A \cdot B$$

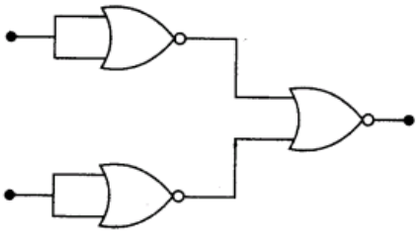
So, the circuit corresponds to AND gate. **(2)**

Symbol



(1)

48.You are given a circuit below. Write its truth table. Hence, identify the logic operation carried out by this circuit. Draw the logic symbol of the gate which corresponds to[All India 2011]



Ans.

$$Z = \overline{A + B} = \bar{\bar{A}} \cdot \bar{\bar{B}} = AB$$

Truth table of given circuit is as shown below:

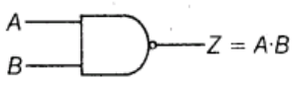
A	B	$X = \bar{A}$	$Y = \bar{B}$	$Z = \overline{X + Y}$
0	0	1	1	0
1	0	0	1	0
0	1	1	0	0
1	1	0	0	1

This circuit carries out by the logic operation of AND gate which can also be verified by De-Morgan's theorem

$$Z = \overline{X + Y} = \overline{\bar{A} + \bar{B}} = \bar{\bar{A}} + \bar{\bar{B}} = A + B = A \cdot B$$

So, the circuit corresponds to AND gate. **(2)**

Symbol



(1)

49.Draw transfer characteristics of a common-emitter n-p-n Point out the region in which the transistor operates as an amplifier.

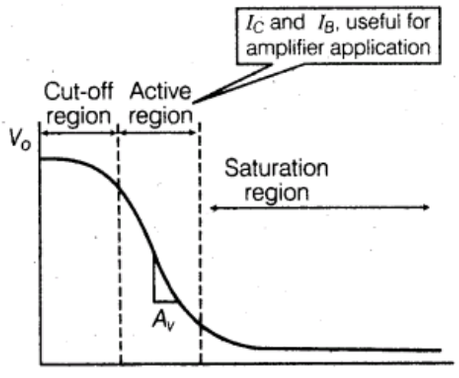
Define the following terms used in transistor amplifiers:

(i)Input resistance

(ii)Output resistance

(iii)Current amplification factor.[Foreign 2011]

Ans.



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}}$$ **(1)**

(*ii*) **Output resistance** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant is called output characteristic curve.

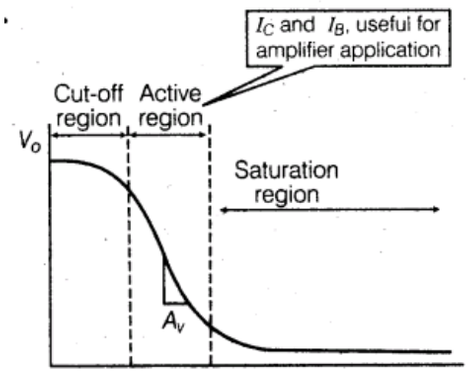
$$\therefore \quad R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

50.Draw the general shape of the transfer characteristics of a transistor in its CE Which regions of this characteristic of a transistor are used when it works as an amplifier?[All India 2010 C]

Ans.



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

(*ii*) **Output resistance** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant is called output characteristic curve.

$$\therefore \quad R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

51.Give the circuit diagram of a common-emitter amplifier using an n-p-n transistor. Draw the input and output wave forms of the signal. Write the expression for its voltage gain. [HOTS,

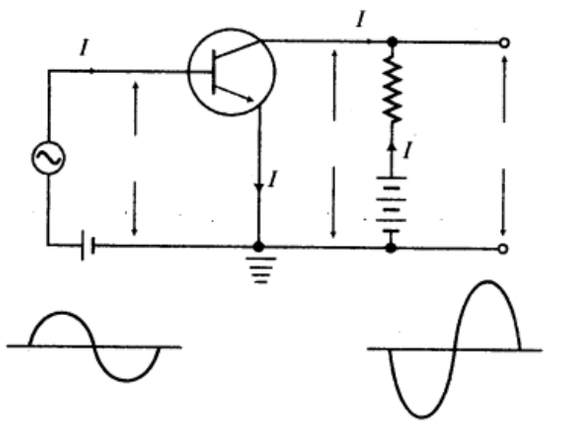
All India 2010]

Ans.

> Whenever CE circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

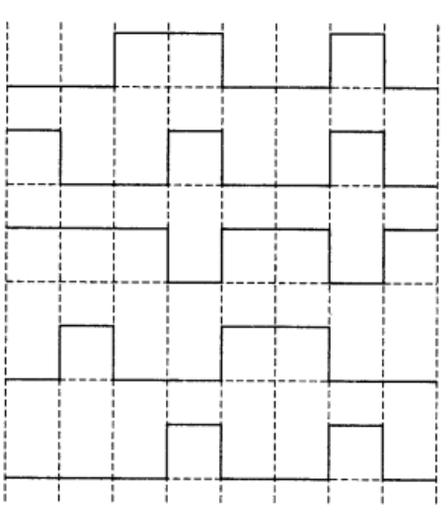
$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C)R_{out}}{\Delta I_B R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

52.The inputs A and B shown here are used as the inputs for three different gates G_1, G_2 and G_3. The outputs obtained in the three cases have the forms shown. Identify the three gates and write their truth tables. [All India 2009 c]



Ans.

For G_1

Gate : NAND gate

Truth table

A	B	$G_1 = \overline{A \cdot B}$
0	0	1
0	1	1
1	0	1
1	1	0

For G_2

Gate : NOR gate

Truth table

A	B	$G_2 = \overline{A + B}$
0	0	1
0	1	0
1	0	0
1	1	0

(1/2 × 2 = 1)

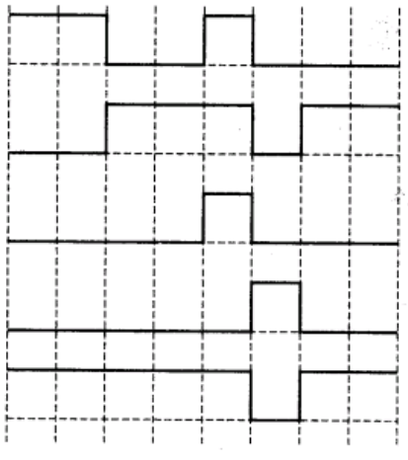
For G_3

Gate : AND gate

Truth table

A	B	$G_3 = A \cdot B$
0	0	0
0	1	0
1	0	0
1	1	1

53.The inputs A and B shown here are used as the inputs for' three different gates G_1, G_2 and G_3 one by one. The outputs obtained in the three cases have the forms shown. Identify the three gates and write their symbols. [All India 2009 C]



Ans.

(*i*) G_1 : AND gate (ii) G_2 : NOR gate

(*iii*) G_3 : OR gate. **(1/2 × 3 = 1½)**

Truth table

A	*B*	G_1	G_2	G_3
0	0	0	1	0
0	1	0	0	1
1	0	0	0	1
1	1	1	0	1

(1½)

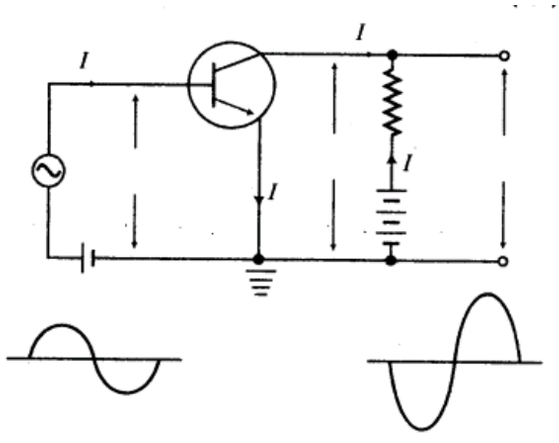
54.Draw the labelled circuit diagram of a common-emitter transistor amplifier. Explain clearly, how the input and output signals are in opposite phase?[All India 2009]

Ans.

Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C)R_{out}}{\Delta I_B\, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

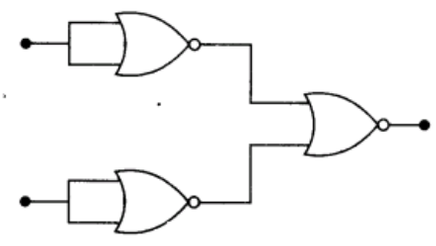
where, β_{AC} is AC current gain.

Relationship between input and output signals of n-p-n transistor amplifier. When positive half cycle is fed into input circuit, forward bias of emitter base circuit decreases. This lead to decrease I_E and by transistor action, collector current decreases.

Since, output voltage, $V_o = V_{CE} - I_C R_L$, therefore, decrease in collector current, increases the output voltage. As, the collector is connected with the negative terminal of battery V_{CC}, the increase in collector voltage imply that negatively of collector increases.

Thus, corresponding to positive half cycle of input AC, a negative amplified cycle is obtained at collector and vice-versa. This shows that output and input signals are in opposite phase

55.The inputs A and B are inverted by using two NOT gates and their outputs are fed to the NOR gate as shown below:
Analyse the action of the gates (1) and (2) and identify the logic gate of the complete circuit so obtained. Give its symbol and the truth table.[All India 2009]



Ans.

The gates 1 and 2 are NOR gates acting as NOT gate.

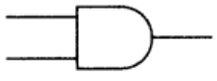
For 1 and 2,

When $A = 0, A = 0, Y = \overline{0 + 0} = \bar{0} = 1$

Similarly, $B = 0, B = 0, Y = \overline{0 + 0} = \bar{0} = 1$ **(1)**

Logic gate of complete circuit AND gate

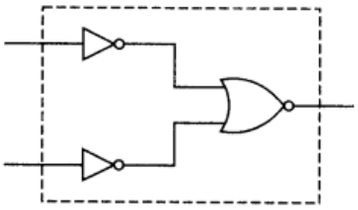
Logic circuit of a AND gate

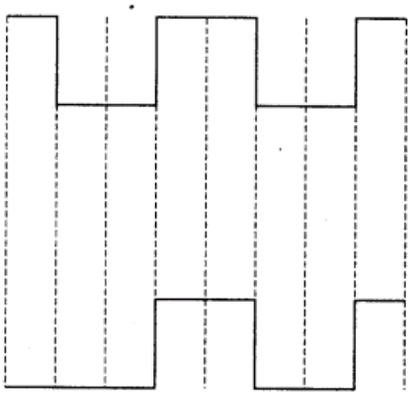


Truth table

A	B	$Y = AB$
0	0	0
0	1	0
1	0	0
1	1	1

56.Identify the gate equivalent to the dotted box shown here and give its symbol and truth table The input A shown here is used with another unknown input B in this set up. If the output Y has the form shown, give the intervals over which the input B is in its high state. [Delhi 2008 C]



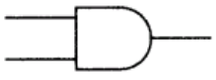


Ans.

$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$

The gate equivalent to dotted box is AND gate. **(1)**

Logic circuit of a AND gate



Truth table

A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1

B is in high state in the interval 3 to 4, 4 to 5 and **7** to **8.**

5 Marks Questions

57.(i) Differentiate between three segments of a transistor on the basis of their size and level of doping.

(ii)How is a transistor biased to be in active state?

(iii)With the help of necessary circuit diagram, describe briefly, how n-p-n transistor in CE configuration amplifies a small sinusoidal input voltage. Write the expression for the AC current gain. [Delhi 2014]

Ans.(i) The base region of the transistor is physically located between the emitter and the collector region and is made from lightly doped high resistivity material. The emitter and collector regions are heavily doped. But the doping level in emitter is slightly greater than that of collector and the area of collector region is slightly more than that of emitter.

In term of doping level,

Emitter region > collector region > base region

In term of area of the region,

Collector region > emitter region > base region.The area of the collector region is greater than that of emitter. This is because the collector region has to handle more power than the emitter and also it has to collect more number of charge carriers to constituent the current. Emitter is heavily doped to provide large member of majority charge carriers, while base and collector are lightly doped to accept these charge carriers from emitter.

(ii) The conditions of a transistor for to be in active state are below:

(a)The input circuit should be forward biased by using a low voltage battery.

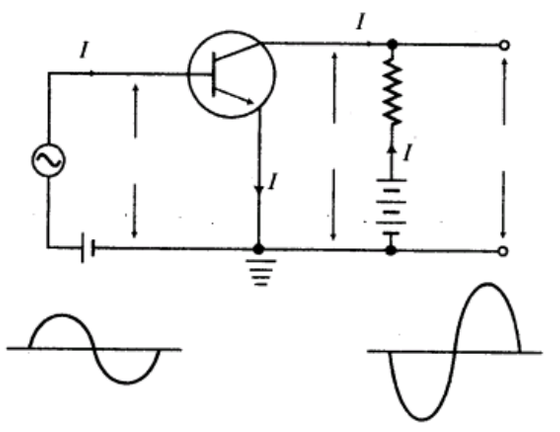
(b)The output circuit should be reverse biased by using a high voltage battery.

(iii) CE configuration While finding gain for CE configuration we should mind that it will depend upon the load resistance, input resistance as well as output will be inverted.

> Whenever CE circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B \, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

Working In the circuit, emitter is forward biased and collector is reversed biased. This makes input resistance (R_{in}) very low and output resistance (R_{out}) high. During the positive half cycle of input AC decrease the forward bias.

Hence, emitter current, I_E and by transistor action collector current decreases. This tend to increase the collector voltage which is given by

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

The high value of R_L produces large change in V_o corresponding to low change in V_i. Thus, amplified pulse is obtained at collector. **(1)**

Voltage gain It is equal to the ratio of change in output voltage (V_{CE}) corresponding to the change in input voltage (ΔV_{BE}), i.e.

$$\text{Voltage gain } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \frac{(\Delta I_C) R_L}{(\Delta I_B) V_i}$$

where, R_L and R_i are output resistances (load resistance) and input resistance of transistor respectively. **(1)**

$$\therefore \quad A_V = \left(\frac{\Delta I_C}{\Delta I_B}\right)\frac{R_L}{r_i} = \beta_{AC}\frac{R_L}{r_i}$$

where, β_{AC} is AC current gain $= \frac{\Delta I_C}{\Delta I_B}$ **(1/2)**

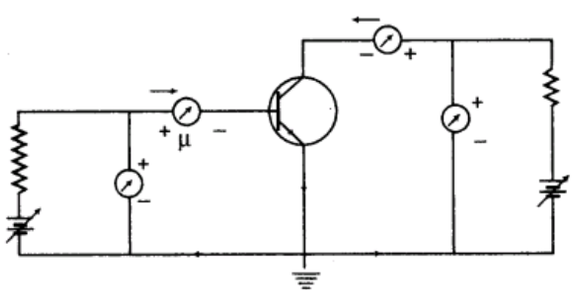
The output voltage of *CE* amplifier differ in phase from the input voltage by 180° or π rad. The opposite phase is represented by negative sign. **(1)**

$$\therefore \quad \text{Voltage gain} = -\beta_{AC}\frac{R_L}{r_i}$$ **(1/2)**

58.(i)Explain briefly with the help of a circuit diagram, how an n-p-n transistor in CE configuration is used to study input and output characteristics.
(ii) Describe briefly the underlying principle of a transistor amplifier working as an oscillator. Hence, use the necessary circuit diagram to explain how self sustained oscillations are achieved in the oscillator. [Delhi 2014 C]

Ans.(i) **Common-emitter Transistor Characteristics**

To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

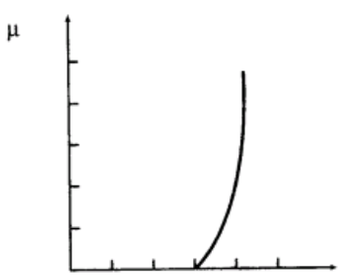
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

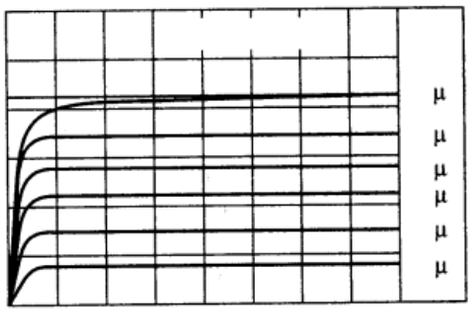
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(*b*) Collector or Output Characteristics

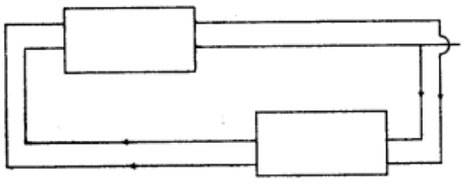
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

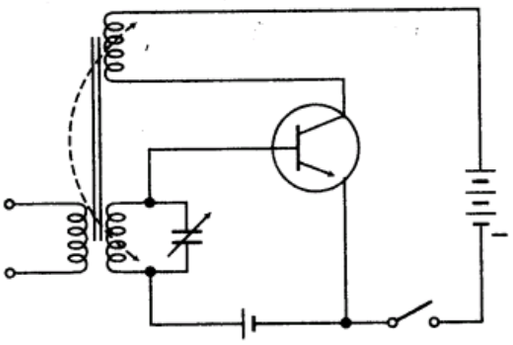
The output characteristics are as shown below:



(ii) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

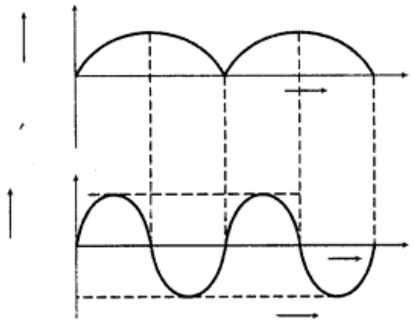


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through **L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

59. (*i*) Draw the circuit diagram of an *n-p-n* transistor with emitter-base junction forward biased and collector-base junction reverse biased. Describe briefly, how the motion of charge carriers in the transistor constitutes the emitter current I_E, the base current I_B and the collector current I_C. Hence, deduce the relation, $I_E = I_B + I_C$.

(*ii*) Explain with the help of a circuit diagram, how a transistor works as an amplifier? **[All India 2014C]**

Ans.(i) In this transistor, the emitter-base junction is forward biased and its resistance is very low. So, the voltage of V_{EE} is quite small.

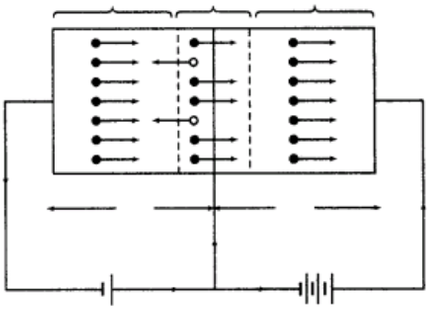
The collector-base junction is reverse biased. The resistance of this junction is very high. So, the voltage of V_{cc} (V_{CB}) is quite large (= 45 V). Electrons in emitter are repelled towards base by negative potential of V_{EE} on emitter, resulting emitter current I_E. The base being thin and

lightly doped has low density of holes, thus when electrons enter the base region, then only a few holes get neutralised by electron hole combination, resulting in base current (I_B). The remaining electrons pass over to the collector, due to high positive potential of collector, resulting in collector current (I_c) . As,' e electron reaches to collector, it gets neutialised by the flow of one electron from the negative terminal of the battery V_{cc} to collector through connecting wire. Then, one electron flow from negative terminal of battery V_{cc} to positive terminal of battery V_{EE} and one electron flow from negative terminal of V_{EE} to emitter.
When the electron coming from emitter combines with the holes in base, then deficiency of hole in the base is compensated by the breaking of covalent bond there. The electron, so released flows to the positive terminal of battery V_{EE}, through connecting wire.
Thus, in n-p-n transistor, the current is carried inside as well as in external circuit by the electrons

Thus, in this case also,

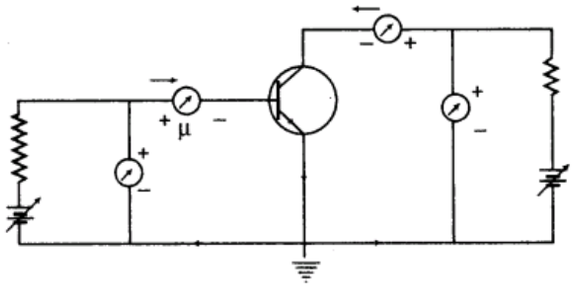
$$I_E = I_B + I_C$$ [Kirchhoff 's first law]

In the base, I_E and I_C flow in opposite direction.



(ii) **Common-emitter Transistor Characteristics**

To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

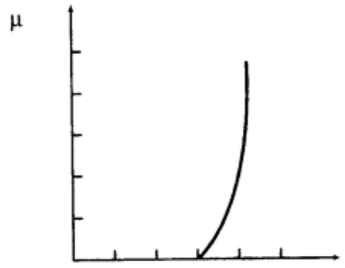
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

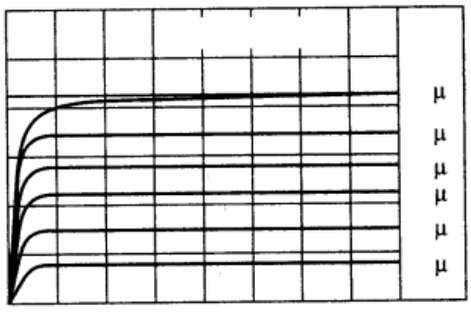
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(*b*) Collector or Output Characteristics

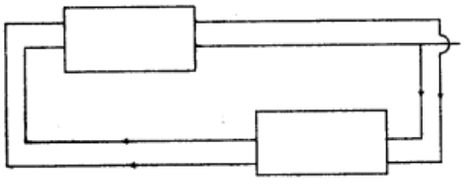
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

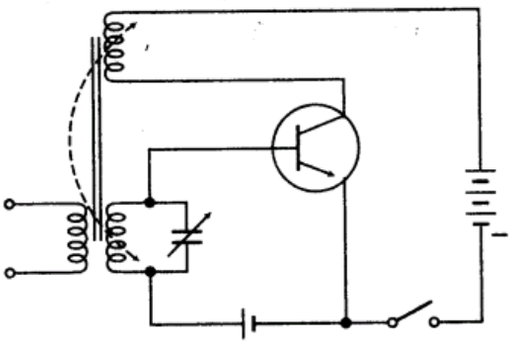
The output characteristics are as shown below:



(c) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

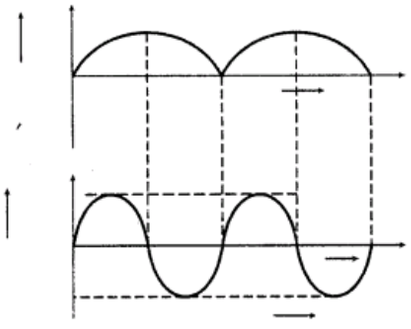


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through**L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

60.(i) Why is the base region of a transistor thin and lightly doped?
(ii) Draw the circuit diagram for studying the characteristics of an n-p-n transistor in common-emitter
configuration.Sketch the typical (a) input and (b) output characteristics in this configuration.
(iii)Describe briefly, how the output characteristics can be used to obtain the current gain in the transistor? [Delhi 2013 C]

Ans.(i) In this transistor, the emitter-base junction is forward biased and its resistance is very low. So, the voltage of V_{EE} is quite small.

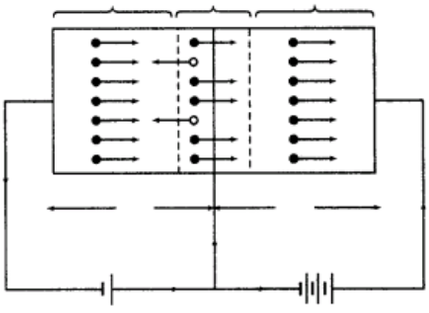
The collector-base junction is reverse biased. The resistance of this junction is very high. So, the voltage of V_{cc} (V_{CB}) is quite large (= 45 V). Electrons in emitter are repelled towards base by negative potential of V_{EE} on emitter, resulting emitter current I_E. The base being thin and lightly doped has low density of holes, thus when electrons enter the base region, then only a few holes get neutralised by electron hole combination, resulting in base current (I_B). The remaining electrons pass over to the collector, due to high positive potential of collector, resulting in collector current (I_C) . As,' e electron reaches to collector, it gets neutialised by the flow of one electron from the negative terminal of the battery V_{cc} to collector through connecting wire. Then, one electron flow from negative terminal of battery V_{cc} to positive

terminal of battery V_{EE} and one electron flow from negative terminal of V_{EE} to emitter.
When the electron coming from emitter combines with the holes in base, then deficiency of hole in the base is compensated by the breaking of covalent bond there. The electron, so released flows to the positive terminal of battery V_{EE}, through connecting wire.
Thus, in n-p-n transistor, the current is carried inside as well as in external circuit by the electrons

Thus, in this case also,

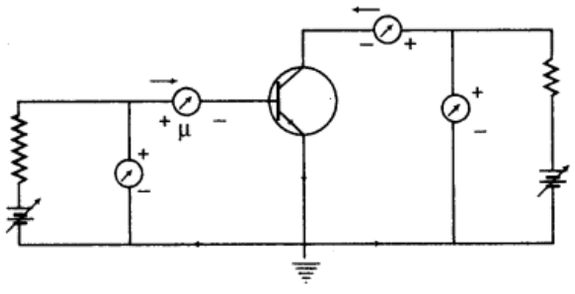
$$I_E = I_B + I_C \quad \text{[Kirchhoff's first law]}$$

In the base, I_E and I_C flow in opposite direction.



(ii) **Common-emitter Transistor Characteristics**

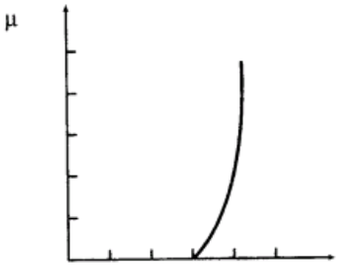
To study the characteristics of an **n-p-n** transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery $\mathbf{V_{cc}}$.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.
These two characteristics can be studied as shown below:

(a) **Emitter or Input Characteristics**

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.
Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.
Now, with the help of rheostat gradually increases, the value of base-emitter voltage $\mathbf{V_{BE}}$ in small steps and note the corresponding values of base current $\mathbf{I_B}$.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

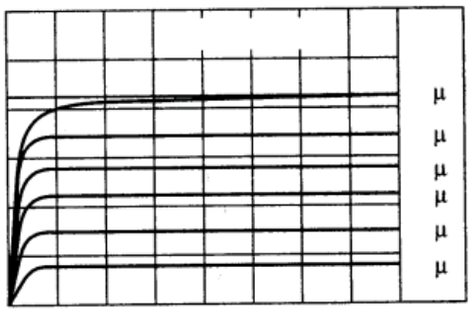
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(*b*) Collector or Output Characteristics

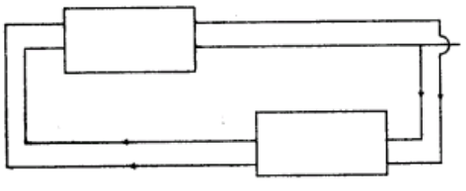
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

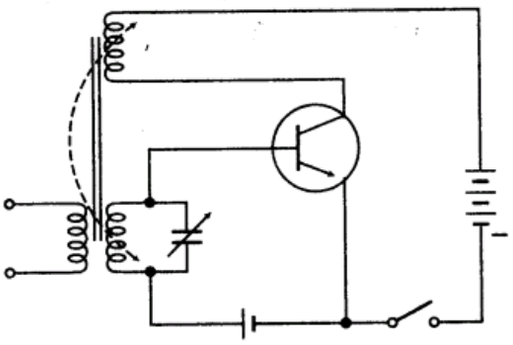
The output characteristics are as shown below:



(c) **Feedback** When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

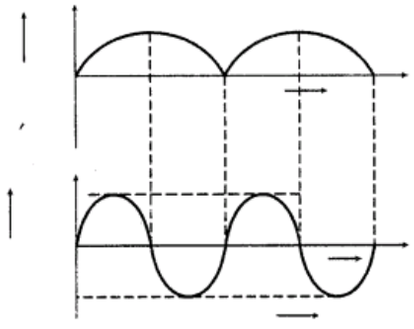


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil **L'** back into input coil **L.** When the switch **K** is closed, collector current begin to flow through **L'**, which in turn increases the magnetic flux linked with **L'** and hence with L This leads to produce an induce emf in **L,** which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through **L'** does not change and therefore flux remains unchanged and emf in **L'** and **L** reduces to zero. Now, the discharging of capacitor begins through **L.** The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil **L** also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle

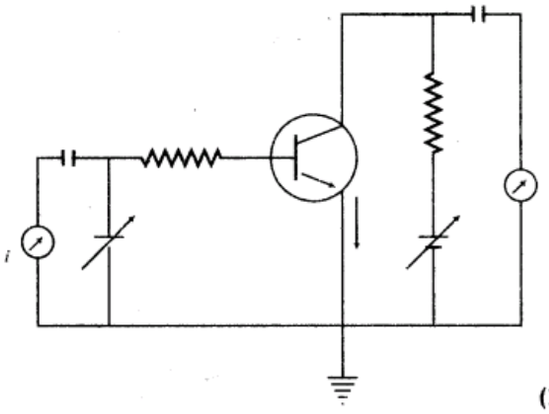


The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B

(iii)**Circuit is as shown below:**

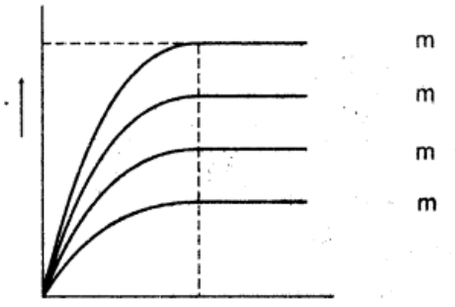


(1)

Current amplification factor (β_{AC}) is the ratio of change in collector current (ΔI_C) to the change is based current (ΔI_B) at constant collector voltage, i.e.

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}} \quad \textbf{(1)}$$

Output characteristics represent the variation of I_C with V_C, keeping I_B constant.

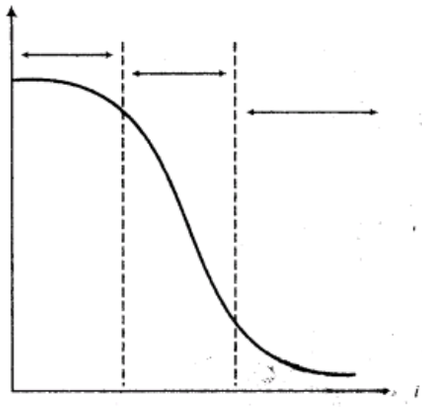


(1)

From above graph at $V_C = V$, the value of collector current increases with the increase in the base current, I_B. Thus,

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}} \quad \text{[AC current gain]}$$

(*ii*) **Transfer characteristics curve for a base-biased transistor in CE configuration.**



(2)

Hence, low input give high output and high input gives low output.

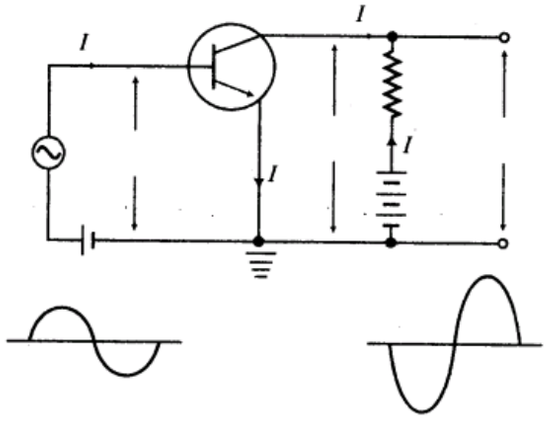
61. Draw a simple circuit of a *CE* transistor amplifier. Explain its working. Show that the voltage gain A_V of the amplifier is given by $A_V = \beta_{AC} R_L / r_i$, where β_{AC} is the current gain, R_L is the load resistance and r_i is the input resistance of the transistor. What is the significance of the negative sign in the expression for the voltage gain. **[HOTS]**

Ans. While finding gain for CE configuration we should mind that it will depend upon the load resistance, input resistance as well as output will be inverted.

> Whenever *CE* circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C) R_{out}}{\Delta I_B \, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

Working In the circuit, emitter is forward biased and collector is reversed biased. This makes input resistance (R_{in}) very low and output resistance (R_{out}) high. During the positive half cycle of input AC decrease the forward bias.

Hence, emitter current, I_E and by transistor action collector current decreases. This tend to increase the collector voltage which is given by

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

The high value of R_L produces large change in V_o corresponding to low change in V_i. Thus, amplified pulse is obtained at collector. **(1)**

Voltage gain It is equal to the ratio of change in output voltage (V_{CE}) corresponding to the change in input voltage (ΔV_{BE}), i.e.

$$\text{Voltage gain } A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}} = \frac{(\Delta I_C)\, R_L}{(\Delta I_B)\, V_i}$$

where, R_L and R_i are output resistances (load resistance) and input resistance of transistor respectively. **(1)**

$$\therefore \quad A_V = \left(\frac{\Delta I_C}{\Delta I_B}\right)\frac{R_L}{r_i} = \beta_{AC}\,\frac{R_L}{r_i}$$

where, β_{AC} is AC current gain $= \dfrac{\Delta I_C}{\Delta I_B}$ **(1/2)**

The output voltage of *CE* amplifier differ in phase from the input voltage by 180° or π rad. The opposite phase is represented by negative sign. **(1)**

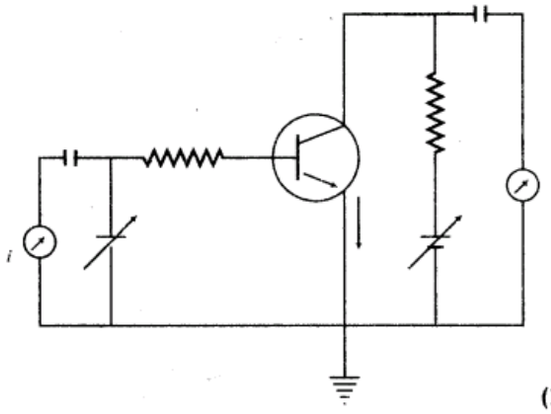
$$\therefore \quad \text{Voltage gain} = -\beta_{AC}\,\frac{R_L}{r_i}$$ **(1/2)**

62. (*i*) Draw the circuit for studying the input and output characteristics of a transistor in *CE* configuration. Show how from the output characteristics the information about the current amplification factor (β_{AC}) can be obtained.

(*ii*) Draw a plot of the transfer characteristics (V_o *versus* V_i) for a base-biased transistor in *CE* configuration.

[All India 2010; Foreign 2012]

Ans.Circuit is as shown below:

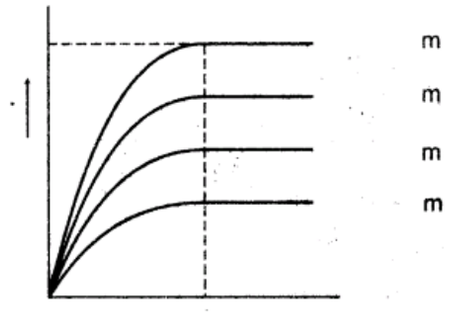


(1)

Current amplification factor (β_{AC}) is the ratio of change in collector current (ΔI_C) to the change is based current (ΔI_B) at constant collector voltage, i.e.

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}} \quad \textbf{(1)}$$

Output characteristics represent the variation of I_C with V_C, keeping I_B constant.

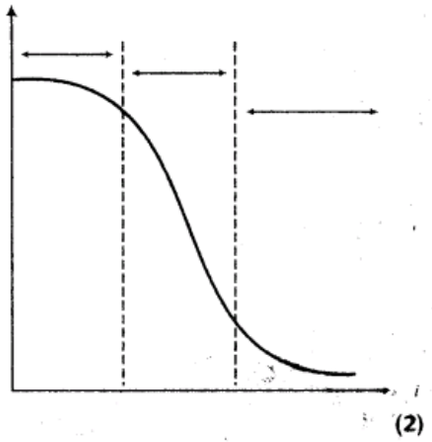


(1)

From above graph at $V_C = V$, the value of collector current increases with the increase in the base current, I_B. Thus,

$$\beta_{AC} = \left.\frac{\Delta I_C}{\Delta I_B}\right|_{V_{CE} = \text{constant}} \quad \text{[AC current gain]}$$

(*ii*) **Transfer characteristics curve for a base-biased transistor in CE configuration.**

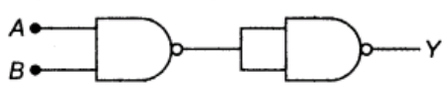


(2)

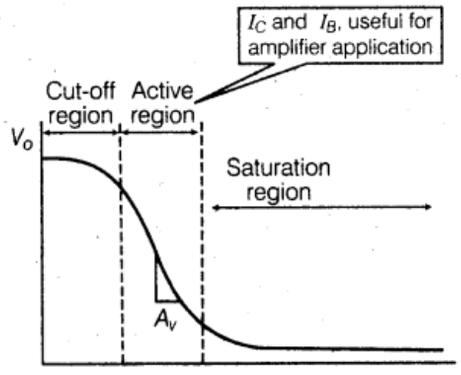
Hence, low input give high output and high input gives low output.

63.(i)Using the necessary circuit diagram, draw the transfer characteristics of a base-biased transistor in CE configuration. With the help of these characteristics, explain briefly how the transistor can be used as an amplifier?

(ii) Why are NAND gate called universal gates? Identify the logical operations carried out by the circuit given as below:



Ans.(i)



(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

(*ii*) **Output resistance** The ratio of variation of collector emitter voltage (V_{CE}) and corresponding change in collector current (ΔI_C) when base current remains constant is called output characteristic curve.

$$\therefore \quad R_{out} = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B\text{ = constant}}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

The active region of a transfer characteristics curve can be used to explain the transistor as an amplifier.

The resistance of output circuit is large being in reverse bias and resistance of input circuit is low being in forward bias.

When input voltage, V_{BE} comes in active region, I_C flows in output and V_o varies significantly as

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

This change in output voltage is obtained as amplified form. **(1)**

(*ii*) NAND gates are termed as universal gates because all three basic gates namely AND, OR and NOT can be made using NAND gate. **(1)**

The given circuit perform the logic operations of AND gate as

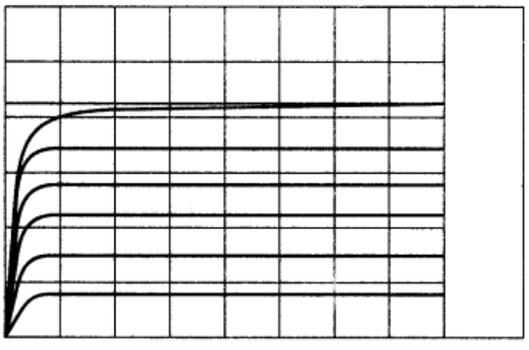
$$Y = \overline{(\overline{A \cdot B})} = A \cdot B \quad \textbf{(1)}$$

64. (*i*) Draw the circuit diagram of a base-biased *n*-*p*-*n* transistor in *CE* configuration. Explain, how this circuit is used to obtain the transfer characteristic V_o - V_i characteristic.

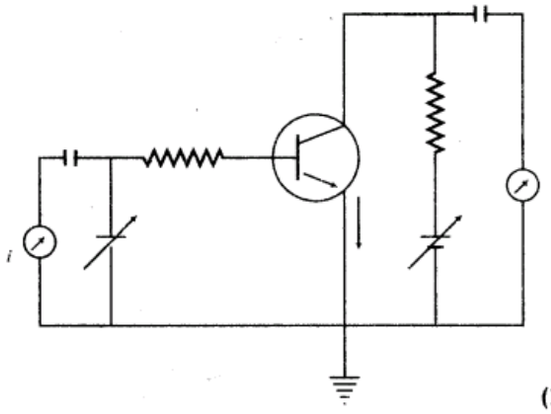
(*ii*) The typical output characteristics I_C *versus* V_{CE} of an *n*-*p*-*n* transistor in *CE* configuration is shown in the figure. Calculate

(*a*) the output resistance r_o and

(*b*) the current amplification factor β_{AC}. **[Foreign 2010]**

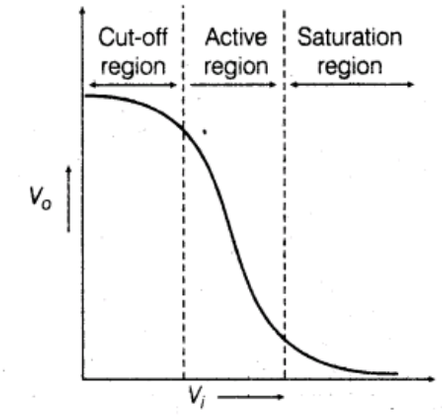


Ans. (i) For n-p-n transistor in CE configuration circuit diagram



(1)

The transfer characteristic curve of base biased transistor in CE configuration as shown below:



(*ii*) (*a*) The output resistance (r_o)

$$= \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

From the given graph, at $I_B = 60\ \mu A$,

$V_{CE} = 2\ V, V_{CE} = 16\ V$

Collector current changes from 8 mA to 8.5 mA,

i.e. $\Delta V_{CE} = 16 - 2 = 14\ V$

$\Delta I_C = 8.5 - 8 = 0.5\ mA = 5 \times 10^{-4}\ A$

$$\therefore \quad r_o = \left(\frac{\Delta V_C}{\Delta I_C}\right)_{I_B = 60\ \mu A} = \frac{14}{5 \times 10^{-4}}$$

$r_o = 2.8 \times 10^4\ \Omega$

$r_o = 28\ k\Omega$ **(1)**

(*b*) The current amplification factor,

$$\therefore \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

At $V_{CE} = 2\ V, I_B = 10\ \mu A$ to $60\ \mu A$

$\therefore \quad \Delta I_B = (60 - 10) = 50\ \mu A$

I_C changes from 1.5 mA to 8 mA

$\therefore \quad \Delta I_C = 8 - 1.5 = 6.5\ mA$

$$\Rightarrow \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \frac{6.5 \times 10^{-3}\ A}{50 \times 10^{-6}\ A}$$

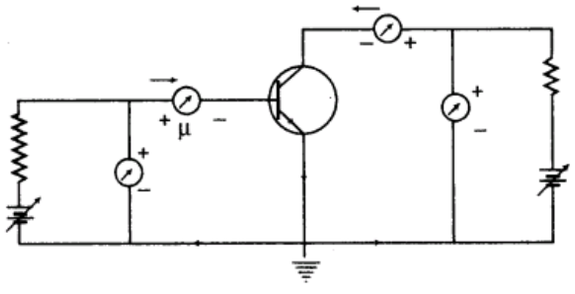
$$\beta_{AC} = \frac{6.5 \times 10^3}{50} = 1.3 \times 10^2$$

$$\Rightarrow \beta_{AC} = 130 \qquad \textbf{(1)}$$

65.(i)Draw the circuit diagram used for studying the input and output characteristics of an n-p-n transistor in the CE configuration. Show the typical shapes of these two characteristics.
(ii) How are the
(a)input resistance
(b)current amplification factor of the transistor determined from these characteristics?
[Delhi 2010 C]

Ans.(i) Common-emitter Transistor Characteristics

To study the characteristics of an n-p-n transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery V_{cc}.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

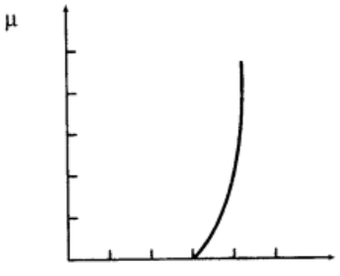
These two characteristics can be studied as shown below:

(a) Emitter or Input Characteristics

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage V_{BE} in small steps and note the corresponding values of base current I_B.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

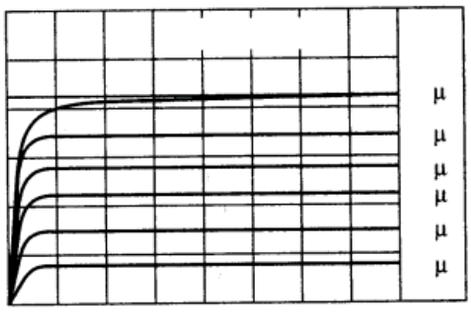
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(*b*) Collector or Output Characteristics

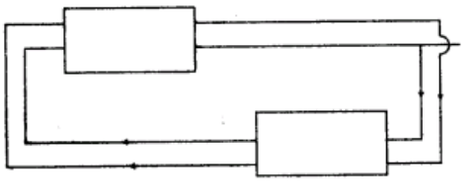
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

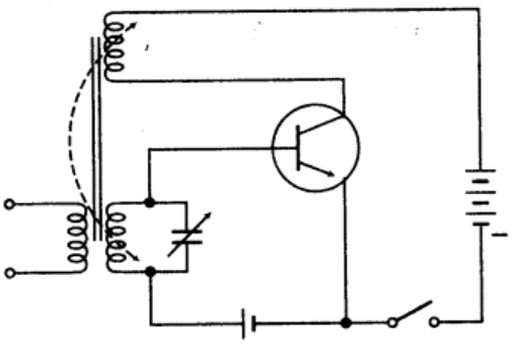
The output characteristics are as shown below:



(ii) Feedback When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

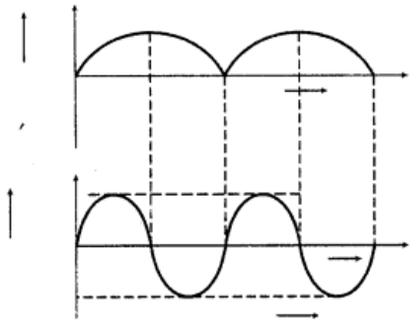


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil L' back into input coil L. When the switch K is closed, collector current begin to flow through //, which in turn increases the magnetic flux linked with L' and hence with L This leads to produce an induce emf in L, which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through L' does not change and therefore flux remains unchanged and emf in L' and L reduces to zero. Now, the discharging of capacitor begins through L. The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil L also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B.

(ii)

(*i*) The input resistance, r_i of transistor in *CE* configuration is defined as the ratio of small change in base-emitter voltage to the corresponding small change in the base current, when the collector emitter voltage is kept constant, i.e.

$$r_i = \left(\frac{\Delta V_{EB}}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

(*ii*) The current amplification factor of a transistor in *CE* configuration is equal to the ratio of the small change in the collector current (ΔI_C) to the small change in base current when collector-emitter voltage is kept constant, i.e.

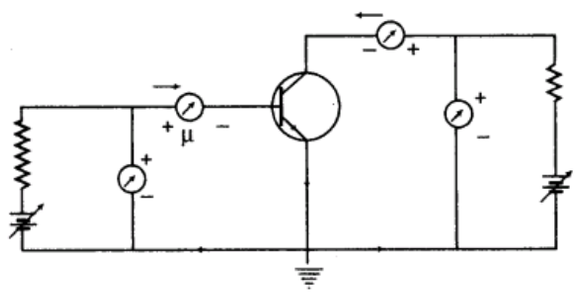
$$\beta = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}\text{ = constant}} \quad \textbf{(1)}$$

66.(i)Draw a circuit diagram to study the input and output characteristics of an n -p- n transistor in its common- emitter configuration. Draw the typical input and output characteristics.

(ii) Explain with the help of a circuit diagram, the working of an n-p-n transistor as a common-emitter amplifier. [Delhi 2009 C]

Ans.(i) Common-emitter Transistor Characteristics

To study the characteristics of an n-p-n transistor in common-emitter mode, required circuit is shown in the figure. Here, base-emitter circuit is forward biased with battery V_{BE} and emitter-collector circuit is reverse biased with battery V_{cc}.



From circuit diagram, we come across to know that it is made up of two sections, i.e. input and output.

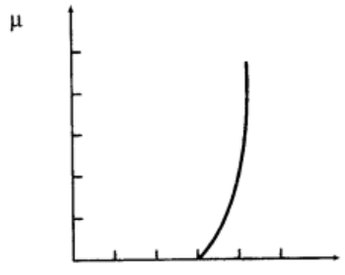
These two characteristics can be studied as shown below:

(a) Emitter or Input Characteristics

A graphical relation between the emitter voltage and the emitter current by keeping collector voltage constant is called input characteristics of the transistor.

Adjust collector-emitter voltage at a suitable high value V_{CE} (say = + 10 V). It is necessary so as to make the base-collector junction reverse biased.

Now, with the help of rheostat gradually increases, the value of base-emitter voltage V_{BE} in small steps and note the corresponding values of base current I_B.



Input resistance It is defined as the ratio of change in base-emitter voltage (ΔV_{BE}) to the resulting change in the base current (ΔI_B) at constant collector-emitter voltage (V_{CE}). It is reciprocal of slope of I_B-V_{BE} curve.

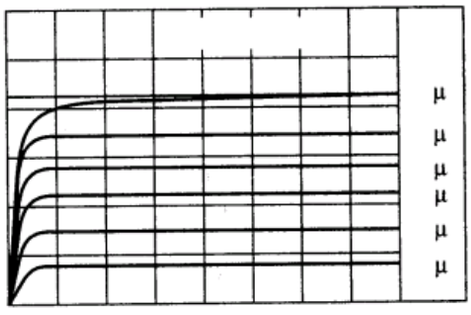
$$\text{Input resistance, } R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

(*b*) **Collector or Output Characteristics**

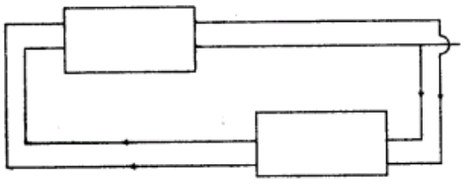
A graphical relation between the collector voltage and collector current by keeping base current constant is called **output characteristics** of the transistor. To study output characteristics of transistor we keep value of base current I_B fixed (say at 10 μA) with the help of V_{BE}. Now, gradually change the value of V_{CE} and note the values of collector current I_C.

Plot I_C V_{CE} graph. Repeat the process for different constant values of I_B.

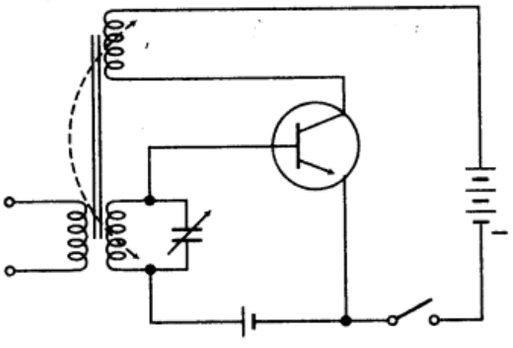
The output characteristics are as shown below:



(ii) Feedback When a portion of the output power is returned back to the input in phase this is termed as positive feedback.

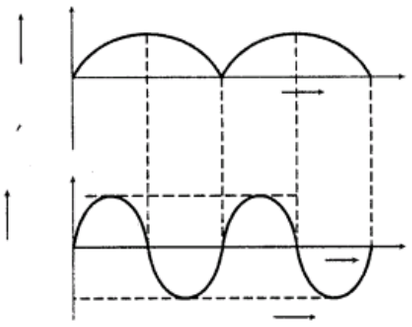


Feedback network The phenomenon of mutual inductance is used to take a part of output in coil L' back into input coil L. When the switch K is closed, collector current begin to flow through //, which in turn increases the magnetic flux linked with L' and hence with L This leads to produce an induce emf in L, which increases the forward bias. This also increases the base current and hence collector current along with the charging of capacitor takes place with upper plate as positive. This phenomenon is repeated again and again till the collector current reaches to its maximum value.



At maximum value of I_C, current through L' does not change and therefore flux remains unchanged and emf in L' and L reduces to zero. Now, the discharging of capacitor begins through L. The positivity of upper plate decreases and forward bias decrease, which results in the form of decrease in base current and hence, decrease in collector current. This phenomenon repeats till collector current reduces to zero and emf in the coil L also reduces to zero.

Thus, the time duration in which collector current grows from zero to maximum, the current in coil L of tank circuit complete its half cycle. The duration in which collector current reduces from maximum to zero, the current in L' completes its next half cycle



The frequency of oscillation is given by

$$\nu = \frac{1}{2\pi\sqrt{LC}}$$

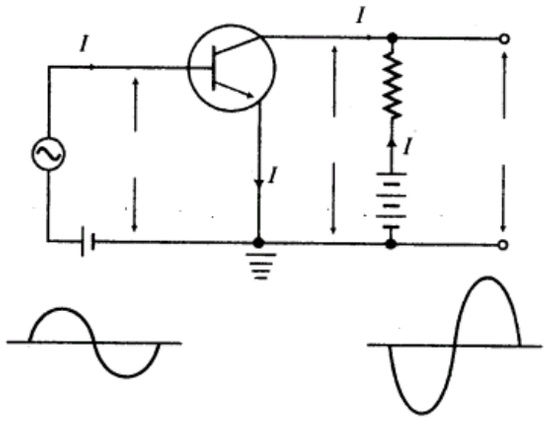
Thus, the AC of desired frequency and amplitude can be obtained by taking appropriate value of inductance,capacitance and strength of battery B.

(ii)

Whenever CE circuit is used as an amplifier the output should be 180° out of phase with the input. The output will also be amplified that is amplitude of output will be more than that of input.

Circuit diagram of a common-emitter amplfier

(1/2)



Voltage gain It is equal to the ratio of small change in output voltage at the collector to that of change in input voltage, i.e.

$$A_V = \frac{\text{Output voltage}}{\text{Input voltage}}$$

$$= \frac{\Delta V_{CE}}{\Delta V_{EB}} = \frac{(\Delta I_C)R_{out}}{\Delta I_B\, R_{in}} = \beta_{AC} \times \frac{R_{out}}{R_{in}} \qquad \left(1\frac{1}{2}\right)$$

$$\Rightarrow \text{ Voltage gain} = \beta_{AC} \times \frac{R_{out}}{B_{in}}$$

where, β_{AC} is AC current gain.

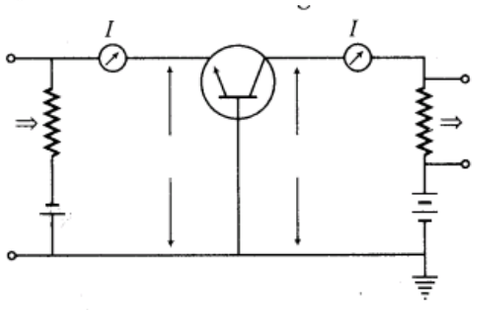
Working of *n-p-n* transistor as *CE* amplifier In the circuit, output resistance is very high whereas input resistance is very low being reverse and forward bias, respectively.

When current, I_C grows in output circuit, potential difference across the collector decreases significantly as per relation

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

When input voltage is fed into input circuit, V_{EB} changes, which in turn change I_B and I_E. By transistor action, I_C change and thus, output voltage changes in amplified manner. **(1)**

67.Draw a circuit diagram of an n-p-n transistor with its emitter base junction forward biased and base- collector junction reverse biased. Describe briefly its working.
Explain, how a transistor in active state exhibits a low resistance at its emitter-base junction and high resistance at its base-collector junction? [Foreign 2009]
Ans. n-p-n transistor in CB configuration
Since, the base is common in input and output circuits, therefore transistor is connected in CB configuration.



(2½)

Working When input voltage, V_{BE} is sufficient to make flow of emitter current, collector current flows in output circuit. In this condition, the circuit is said to be in active state.
The small change in V_{EB}, produces sufficient change in emitter current and hence, in collector current. The input circuit offers very small resistance as ample change in emitter current occurs corresponding to small change in input voltage.
This lead to produce large change in output voltage inspite of smaller change in collector current ($I_E < I_C$). This shows that output circuit offer high resistance

68.Draw a labelled circuit diagram of a base-biased transistor in common-emitter configuration. Plot the transfer characteristics of this base biased transistor indicating the different regions of its operation.[Delhi 2009 c]
Ans.

(*ii*) (*a*) The output resistance (r_o)

$$= \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B = \text{constant}}$$

From the given graph, at $I_B = 60\ \mu A$,

$V_{CE} = 2\ V, V_{CE} = 16\ V$

Collector current changes from 8 mA to 8.5 mA,

i.e. $\Delta V_{CE} = 16 - 2 = 14\ V$

$\Delta I_C = 8.5 - 8 = 0.5\ mA = 5 \times 10^{-4}\ A$

$$\therefore \quad r_o = \left(\frac{\Delta V_C}{\Delta I_C}\right)_{I_B = 60\ \mu A} = \frac{14}{5 \times 10^{-4}}$$

$r_o = 2.8 \times 10^4\ \Omega$

$r_o = 28\ k\Omega$ **(1)**

(*b*) The current amplification factor,

$$\therefore \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

At $V_{CE} = 2\ V, I_B = 10\ \mu A$ to $60\ \mu A$

$\therefore \quad \Delta I_B = (60 - 10) = 50\ \mu A$

I_C changes from 1.5 mA to 8 mA

$\therefore \quad \Delta I_C = 8 - 1.5 = 6.5\ mA$

$$\Rightarrow \quad \beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE}} = \frac{6.5 \times 10^{-3}\ A}{50 \times 10^{-6}\ A}$$

$$\beta_{AC} = \frac{6.5 \times 10^3}{50} = 1.3 \times 10^2$$

$\Rightarrow \quad \beta_{AC} = 130$ **(1)**

69. (*i*) Draw the circuit arrangement needed for studying the input and output characteristics of an *n-p-n* transistor in its common- emitter configuration. Draw the typical shape of these input and output characteristics. Why is it, that it is usually enough to determine only one input characteristic?

(*ii*) The small signal current gain β_{AC} of a transistor can be taken as nearly equal to its DC current amplification factor β_{DC}. Why?

[All India 2008C]

Ans.(i)

The active region of a transfer characteristics curve can be used to explain the transistor as an amplifier.

The resistance of output circuit is large being in reverse bias and resistance of input circuit is low being in forward bias.

When input voltage, V_{BE} comes in active region, I_C flows in output and V_o varies significantly as

$$V_o = V_{CE} = V_{CC} - I_C R_L$$

This change in output voltage is obtained as amplified form. **(1)**

(*ii*) NAND gates are termed as universal gates because all three basic gates namely AND, OR and NOT can be made using NAND gate. **(1)**

The given circuit perform the logic operations of AND gate as

$$Y = \overline{\overline{(A \cdot B)}} = A \cdot B \quad \textbf{(1)}$$

(*ii*) The AC current gain is equal to the ratio of change of collector current to the corresponding change in base current at given collector emitter voltage, i.e.

$$\beta_{AC} = \left(\frac{\Delta I_C}{\Delta I_B}\right)_{V_{CE} = \text{constant}}$$

and $$\beta_{DC} = \left(\frac{I_C}{I_B}\right)_{V_{CE} = \text{constant}} \quad \textbf{(1)}$$

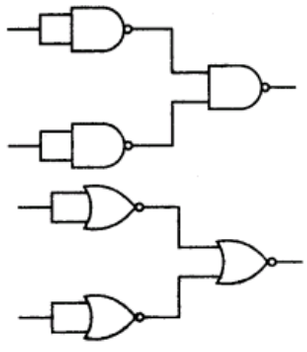
Therefore, β_{AC} is nearly equal to β_{DC}. **(1)**

70.(i) The same input -a! is applied to both the (input) terminals of a given logic gate. If the output is(a)same as the (common) input signal.

(b)inverted with respect to the (common) input signal.

Identify the logic gates involved in each case.

(ii) Write the truth tables for each of the combinations shown below. Also identify the logic operations performed by them. [All India 2008 C]

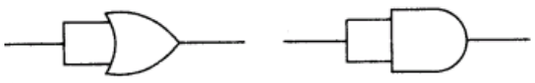


Ans.

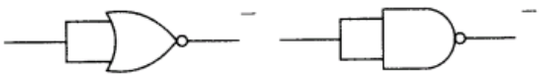
(*i*) (*a*) The logic gate involved may be OR or AND gate as for,

$A = B = 0$ or $A = B = 1$ **(1/2)**

$Y = D$ or 1 is OR and AND gate



(*ii*) The logic gate involved, may be NOR or NAND gates.



(1)

(*ii*) (*a*) The logic operation performed by the combination of gates is of OR gate

$$Y = \overline{\overline{A} \cdot \overline{B}} = A + B$$ **(1)**

Truth table

A	***B***	***Y = A + B***
0	0	0
0	1	1
1	0	1
1	1	1

(1/2)

(*b*) The logic operation performed by the combination of gates is of AND gate

$$Y = \overline{\overline{A} + \overline{B}} = A \cdot B$$ **(1/2)**

Truth table

A	***B***	***Y***
0	0	0
0	1	0
1	0	0
1	1	1